

February 9, 2004

To: Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/718,865 11/21/03

Simon Chooi et al.

A METHOD TO CREATE A COPPER  
DIFFUSION DETERRENT INTERFACE

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450, on February 9, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 2/17/04

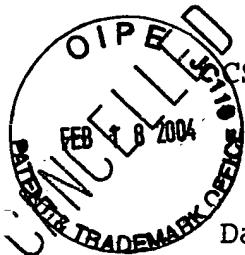
U.S. Patent 5,933,758 to Jain, "Method for Preventing Electroplating of Copper on an Exposed Surface at the Edge Exclusion of a Semiconductor Wafer", teaches a barrier layer over a dual damascene opening.

U.S. Patent 5,693,563 to Teong, "Etch Stop for Copper Damascene Process", discusses dual barrier layers in a dual damascene process.

U.S. Patent 5,451,542 to Ashby, "Surface Passivation Process of Compound Semiconductor Material Using UV Photosulfidation", teaches an S surface passivation process.

The following two U.S. Patents teach the use of a copper sulfide on copper wiring:

- 1) U.S. Patent 5,953,628 to Kawaguchi, "Method for Forming Wiring for a Semiconductor Device".
- 2) U.S. Patent 5,863,834 to Kawaguchi et al., "Semiconductor Device and Method of Manufacturing the Same."



CS-99-332B



U.S. Patent 6,040,243 to Li et al., "Method to Form Copper Damascene Interconnects Using a Reverse Barrier Metal Scheme to Eliminate Copper Diffusion," discloses a method of fabricating damascene vias.

U.S. Patent 6,335,570 to Mori et al., "Semiconductor Device and Manufacturing Method Thereof," discloses a semiconductor device capable of preventing diffusion of a particle of copper or the like which forms a conductive layer without any increase in the number of manufacturing steps.

Sincerely,

Stephen B. Ackerman,  
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION  
(Use several sheets if necessary)

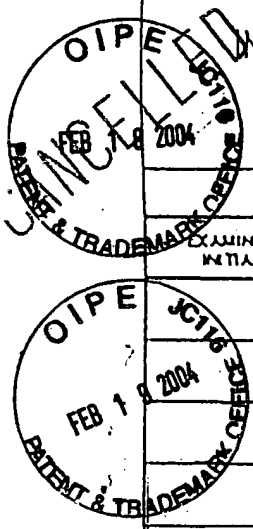
DocId: Number (Specimen)  
CS-99-332B

Application Number  
10/718,865

Applicant  
Simon Chooi et al.

Filing Date  
11/21/03

Group Art Unit



U. S. PATENT DOCUMENTS											
EXAMINER INITIAL	DOCUMENT NUMBER						DATE	NAME	CLASS	SUBCLASS	PLUNG DATE IF APPROPRIATE
JG116 2004 TRADEMARK OFFICE	5	9	3	3	7	5	8/3/99	Jain	438	687	5/12/97
	5	6	9	3	5	6	3/12/97	Teang	437	190	7/15/96
	5	4	5	1	5	4	2/9/95	Ashby	437	173	6/21/94
	5	9	5	3	6	2	8/9/99	Kawaguchi	438	635	1/27/98
	5	8	6	3	8	3	4/1/26/99	Kawaguchi et al.	438	625	3/4/97
	6	0	4	0	2	4	3/3/21/00	Li et al.	438	687	9/20/99
	6	3	3	5	5	7	0/1/10/02	Mori et al.	257	751	4/20/99

FOREIGN PATENT DOCUMENTS												
	DOCUMENT NUMBER						DATE	COUNTRY	CLASS	SUBCLASS	Translation	
											YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Part/next Pages, Etc.)									

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.



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ASSOCIATE POWER OF ATTORNEY

I hereby appoint Cheryl R. Figlin, registration number 39,562, as my associate attorney in this case. Her telephone number is (610) 821-0414.

Please continue to direct all correspondence in this case to the undersigned attorney.

Respectfully submitted,

Stephen B. Ackerman,

Principal attorney of record